Amendments to the Claims

Claims 1-71 (Cancelled)

72. (New) A cubic memory array, comprising,

a substrate;

a plurality of levels of memory cells formed on the substrate one level upon the other, the memory cells of each level are substantially aligned with memory cells in the adjacent level;

a plurality of sets of first select lines formed in each of the plurality of levels of memory cells substantially parallel to the substrate; and

a plurality of sets of second select lines formed in planes orthogonal to the substrate;

wherein each of the memory cells is adjacent to a respective first and second select line.

73. (New) The cubic memory array of claim 72, wherein at least one of the memory cells stores multiple states allowing for more than one bit of information in the memory cell.

74. (New) The cubic memory array of claim 72, wherein at least one of the memory cells includes an antifuse device.

75. (New) The cubic memory array of claim 72, wherein at least one of the memory cells includes a tunnel junction device.

76. (New) The cubic memory array of claim 72, wherein at least one of the memory cells includes,

a storage device having a first cross-sectional area;

a control element in series with the storage device and having a second cross-sectional area greater than the first cross-sectional area.

77. (New) The cubic memory array of claim 72, wherein the plurality of sets of second select lines are formed of tungsten.

78. (New) The cubic memory array of claim 72, wherein at least one of the memory cells includes an angled storage element patterned to create an enhanced electric field.

79. (New) The cubic memory array of claim 72, wherein at least one of the memory cells has dual storage elements and wherein only one storage element is used.

80. (New) The cubic memory array of claim 72, wherein the plurality of sets of first select lines are formed in at least a partial serpentine pattern.

81. (New) The cubic memory array of claim 72, where at least one of the plurality of sets of second select lines are formed from an array of sub-pillars connected by a subset of second select lines formed parallel to the substrate surface.

82. (New) A cubic memory array, comprising:

a substrate;

a first plane of an array of memory cells disposed on the substrate;

a first set of select lines forming rows of memory cells on the first plane;

a second plane of an array of memory cells disposed on the first plane and aligned with the array of memory cells of the first plane;

a second set of select lines orthogonal to the planer surface interconnecting the first and second planes of memory cells wherein each memory cell is adjacent to one of the first set of select lines and adjacent to one of the orthogonal second set of select lines.

83. (New) The cubic memory array of claim 82, wherein at least one of the memory cells stores multiple states allowing for more than one bit of information in the memory cell.

84. (New) The cubic memory array of claim 82, wherein at least one of the memory cells includes an antifuse device.

85. (New) The cubic memory array of claim 82, wherein at least one of the memory cells includes a tunnel junction device.

86. (New) The cubic memory array of claim 82, wherein at least one of the memory cells includes,

a storage device having a first cross-sectional area;

a control element in series with the storage device and having a second cross-sectional area greater than the first cross-sectional area.

87. (New) The cubic memory array of claim 82, wherein the second set of select lines are formed of tungsten.

88. (New) The cubic memory array of claim 82, wherein at least one of the memory cells includes an angled storage element patterned to create an enhanced electric field.

89. (New) The cubic memory array of claim 82, wherein at least one of the memory cells has dual storage elements and wherein only one storage element is used.

90. (New) The cubic memory array of claim 82, wherein the first set of select lines are formed in at least a partial serpentine pattern.

91. (New) The cubic memory array of claim 82, where at least one of the second set of select lines are formed from an array of sub-pillars connected by a subset of second select lines formed parallel to the substrate surface.

92. (New) A cubic memory array, comprising:

a plurality of horizontal select lines;

a plurality of vertical select lines;

a plurality of memory cells, each memory cell adjacent to a horizontal select line and adjacent to a vertical select line;

wherein the plurality of memory cells are arranged to form planes of horizontal select lines and planes of vertical select lines orthogonal to each other.

93. (New) The cubic memory array of claim 92, wherein at least one of the memory cells stores multiple states allowing for more than one bit of information in the memory cell.

94. (New) The cubic memory array of claim 92, wherein at least one of the memory cells includes an antifuse device.

95. (New) The cubic memory array of claim 92, wherein at least one of the memory cells includes a tunnel junction device.

96. (New) The cubic memory array of claim 92, wherein at least one of the memory cells includes,

a storage device having a first cross-sectional area;

a control element in series with the storage device and having a second cross-sectional area greater than the first cross-sectional area.

97. (New) The cubic memory array of claim 92, wherein the vertical select lines are formed of tungsten.

98. (New) The cubic memory array of claim 92, wherein at least one of the memory cells includes an angled storage element patterned to create an enhanced electric field.

99. (New) The cubic memory array of claim 92, wherein at least one of the memory cells has dual storage elements and wherein only one storage element is used.

100. (New) The cubic memory array of claim 92, wherein the horizontal of select lines are formed in at least a partial serpentine pattern.

101. (New) The cubic memory array of claim 92, where at least one of the vertical select lines are formed from an array of sub-pillars connected by a subset of second horizontal select lines.

102. (New) A cubic memory array, comprising:

a substrate having a first surface

a horizontal bit line disposed parallel to first surface of the substrate;

an isolation layer formed on a portion of the horizontal bit line;

a vertical bit line formed next to the isolation layer and contacting the horizontal bit line;

a first memory cell having,

a storage element adjacent to the vertical bit line,

a control element in series with the storage element, and

a first horizontal word line disposed on the isolation layer and contacting the control element; and

at least one additional memory cell having a second horizontal word line disposed on the first memory cell and contacting the vertical bit line.

103. (New) The cubic memory array of claim 102, wherein at least one of the storage elements stores multiple states allowing for more than one bit of information in the storage element.

104. (New) The cubic memory array of claim 102, wherein at least one of the storage elements is an antifuse device.

105. (New) The cubic memory array of claim 102, wherein at least one of the storage cells is a tunnel junction device.

106. (New) The cubic memory array of claim 102, wherein

the storage device has a first cross-sectional area;

the control element has a second cross-sectional area greater than the first cross-sectional area.

107. (New) The cubic memory array of claim 102, wherein the vertical bit line comprises tungsten.

108. (New) The cubic memory array of claim 102, wherein the storage element comprises an angled storage element patterned to create an enhanced electric field.

109. (New) The cubic memory array of claim 102, wherein the memory cells has an additional storage element and wherein the additional storage element is not used to store information.

110. (New) The cubic memory array of claim 102, wherein the horizontal bit line is formed in at least a partial serpentine pattern.

111. (New) The cubic memory array of claim 102, where the vertical bit line is formed from an array of sub-pillars connected by a subset of second horizontal bit lines.

112. (New) A cubic memory array, comprising:

a plurality of horizontal bit lines;

a plurality of sets of stacked memory cells, each set disposed on one of the plurality of horizontal bit lines;

a plurality of vertical bit lines positioned and contacting the plurality of horizontal bit lines, the vertical bit lines also contacting the plurality of stacked memory cells; and

a plurality of horizontal word lines orthogonal to the vertical bit lines and contacting the plurality of sets of stacked memory cells.

113. (New) The cubic memory array of claim 112, wherein at least one of the stacked memory cells includes a storage element that stores multiple states allowing for more than one bit of information in the storage element.

114. (New) The cubic memory array of claim 112, wherein at least one of the stacked memory cells comprises an antifuse device.

115. (New) The cubic memory array of claim 112, wherein at least one of the stacked memory cells comprises a tunnel junction device.

116. (New) The cubic memory array of claim 112, wherein at least one of the stacked memory cells comprises,

a storage device having a first cross-sectional area;

a control element having a second cross-sectional area greater than the first cross-sectional area.

117. (New) The cubic memory array of claim 112, wherein at least one of the plurality of vertical bit lines comprises tungsten.

118. (New) The cubic memory array of claim 112, wherein at least one of the stacked memory storage cells comprises an angled storage element patterned to create an enhanced electric field.

119. (New) The cubic memory array of claim 112, wherein the stacked memory cells has an additional storage element and wherein the additional storage element is not used.

120. (New) The cubic memory array of claim 112, wherein one of the plurality of horizontal word lines is formed in at least a partial serpentine pattern.

121. (New) The cubic memory array of claim 112, where at least one of plurality of vertical bit line is formed from an array of sub-pillars connected by a subset of horizontal bit lines.

122. (New) A cubic memory array, comprising

a first horizontal select line;

a first set of memory cells adjacent to the first horizontal select line;

a first set of vertical select lines intersecting with the first set of memory cells;

a second horizontal select line isolated from the first set of memory cells;

a second set of memory cells adjacent to the second horizontal select line;

a second set of vertical select lines intersecting with the second set of memory cells;

a third horizontal select line isolated from and stacked upon the first horizontal select line;

a third set of memory cells adjacent to the third horizontal select line;

a fourth horizontal select line isolated from and stacked upon the second horizontal select line; and

a forth set of memory cells adjacent to the fourth horizontal select line;

wherein the first set of vertical select lines intersect with the third set of memory cells, and the second set of vertical select lines intersect with the fourth set of memory cells.

123. (New)The cubic memory array of claim 122, further comprising:

control circuitry in the substrate including a set of control elements, the control elements connected to a respective vertical select line.

124. (New) The cubic memory array of claim 122, further comprising:

control circuitry;

control elements disposed on top of the vertical select lines;

a set of horizontal bitlines connecting the control elements to the control circuitry.

125. (New) The cubic memory array of claim 122, wherein at least one of the memory cells includes a storage element that stores multiple states allowing for more than one bit of information in the storage element.

126. (New) The cubic memory array of claim 122, wherein at least one of the memory cells comprises an antifuse device.

127. (New) The cubic memory array of claim 122, wherein at least one of the memory cells comprises a tunnel junction device.

128. (New) The cubic memory array of claim 122, wherein at least one of the memory cells comprises,

a storage device having a first cross-sectional area;

a control element having a second cross-sectional area greater than the first cross-sectional area.

129. (New) The cubic memory array of claim 122, wherein at least one of the vertical select lines comprises tungsten.

130. (New) The cubic memory array of claim 122, wherein at least one of the memory storage cells comprises an angled storage element patterned to create an enhanced electric field.

131. (New) The cubic memory array of claim 122, wherein the memory cells has an additional storage element and wherein the additional storage element is not used.

132. (New) A cubic memory array, comprising:

a substrate;

a set of horizontal word lines formed parallel to the substrate in a plurality of layers;

a set of top sub-column connects;

a set of bottom sub-column connects, the top and bottom sub-column connects parallel to the substrate and orthogonal to the set of horizontal word lines;

wherein the vertical bit lines are formed in more than one pillar and are interconnected by one of the set of top sub-column connects and one of the set of bottom sub-column connects;

wherein the every other pillar is connected to one of a top sub-column connect or a bottom sub-column connect; and

a set of memory cells, each memory cell having,

a storage element adjacent to a pillar,

a control element in series with the storage element connected to a horizontal word line.

133. (New) The cubic array of claim 132, further comprising:

a substrate;

control circuitry having control elements formed in the substrate;

a set of horizontal bit lines, each interconnected to every other pillar using the control elements to select a desired pillar.

134. (New) The cubic memory array of claim 132, wherein at least one of the storage elements stores multiple states allowing for more than one bit of information in the storage element.

135. (New) The cubic memory array of claim 132, wherein at least one of the storage elements is an antifuse device.

136. (New) The cubic memory array of claim 132, wherein at least one of the storage cells is a tunnel junction device.

137. (New) The cubic memory array of claim 132, wherein

the storage device has a first cross-sectional area;

the control element has a second cross-sectional area greater than the first cross-sectional area.

138. (New) The cubic memory array of claim 132, wherein the vertical bit line comprises tungsten.

139. (New) The cubic memory array of claim 132, wherein the storage element comprises an angled storage element patterned to create an enhanced electric field.

140. (New) The cubic memory array of claim 132, wherein the memory cells has an additional storage element and wherein the additional storage element is not used to store information.

141. (New) The cubic memory array of claim 132, wherein the horizontal word line is formed in at least a partial serpentine pattern.